

## CALIBRATED FULLY DIFFERENTIAL RC FILTER

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] Not Applicable

## STATEMENT OF FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

5 [0002] Not Applicable

## BACKGROUND OF THE INVENTION

## 1. TECHNICAL FIELD

[0003] This invention relates in general to electronic circuits and, more particularly, to RC filters.

## 10 2. DESCRIPTION OF THE RELATED ART

[0004] RC-active filters need calibration because of the poor control on the absolute values of integrated resistors and capacitors. In CMOS technologies, these spreads may produce variations in the RC products as high as  $\pm 50\%$ . State-of-the-art processes have high-poly resistance spreads in the range  $225\text{--}425\Omega/\square$  ( $\pm 30\%$ ) and the poly1-poly2 capacitance in the range  $1.15\text{--}1.65\text{fF}/\mu\text{m}^2$  ( $\pm 17\%$ ).

15

[0005] In general, an RC-active filter must have a fairly precise, and predictable, filtering curve. Variations in the RC products due to technology spreads have a strong impact on the shape of the filter. The possible variation in

filter shape due to variations in the RC product is usually not acceptable and thus filter calibration is often mandatory.

[0006] A technique for automatically tuning integrated circuit RC-active filters is set forth in J.B. Hughes, N.C. Bird, and R.S. Sohn, *Self-Tuned RC-Active*  
5 *Filters for VLSI*, Electronic Letters, 11<sup>th</sup> September 1986, Vol. 22, No. 19, paper 6-6 (hereinafter "*Hughes*"). This paper proposes a separate on-chip monitor circuit to evaluate and tune the RC product of an RC-active filter using adjustable capacitor arrays. However, this filter has an asymmetrical coverage range (-33% to +100%) that does not cover all the entire theoretical RC product variation  
10 range.

[0007] Therefore, a need exist for an RC-active filter with a range that covers all product variations.

## BRIEF SUMMARY OF THE INVENTION

[0008] In the present invention, a calibrated filter comprises an RC filter having tunable capacitors having a capacitive value responsive to a control code, a fully differential calibration circuit and a logic circuit. The calibration circuit

5 comprises a differential operational amplifier, a differential voltage source, a first resistor selectively coupled between a first terminal of the differential voltage source and a first integrating capacitor coupled across a first input and a first output of the differential operational amplifier, and a second resistor selectively coupled between a second terminal of the differential voltage source and a

10 second integrating capacitor coupled across a second input and a second output of the differential operational amplifier. The logic circuit charges the first and second capacitors through the first and second resistors over a first predetermined number of clock periods and discharging the integrating capacitors by a predetermined voltage over a second predetermined number of

15 clock periods. A control code for tuning the tunable capacitors by counting the number of clock periods to needed to discharge the integrating capacitors to a predetermined voltage level.

## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0009] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

5 [0010] Figure 1a illustrates a block diagram of a calibrated fully differential RC filter;

[0011] Figure 1b illustrates a schematic representation of a tunable capacitor array;

10 [0012] Figure 2 illustrates a schematic representation of a calibration circuit;

[0013] Figure 3 illustrates a timing diagram of the calibration circuit of Figure 2;

[0014] Figures 4a through 4c illustrate the calibration circuit of Figure 2 at different modes of the timing diagram of Figure 3;

15 [0015] Figure 5 shows the behavior of the calibration system in all tuning conditions ( $RC_{MIN}$ ,  $RC_{NOM}$ ,  $RC_{MAX}$ );

[0016] Figure 6 illustrates the timing signals for the finite state machine of Figure 1a; and

20 [0017] Figure 7 illustrates a Butterworth RC filter that could be used as the RC filter in Figure 1a.

## Detailed Description of the Invention

[0018] The present invention is best understood in relation to Figures 1-7 of the drawings, like numerals being used for like elements of the various drawings.

5 [0019] Figure 1a illustrates a block diagram of a calibrated RC filter 4. An RC filter 6 uses tunable capacitor arrays 7 (see Figure 1b) in its design to compensate for processing variations. The tunable capacitor arrays 7 are set by a finite state machine (FSM) 8 according to values determined through use of a calibration circuit 10.

10 [0020] Figure 1b illustrates a schematic of a tunable capacitor array 7. Each tunable capacitor array 7 uses a plurality of binary-weighted capacitors 9 that can be selectively enabled or disabled responsive to a control word from the finite state machine 8. Accordingly, the capacitance can be varied from a minimal capacitance (one capacitor 9 enabled) to a maximum capacitance (all  
15 capacitors 9 enabled) with a nominal center value equal to the design value of the capacitor. The range of the capacitor array 7 is as great as the combined spread of the resistors and capacitors (i.e.,  $\pm 47\%$  for the previously specified processing technology).

[0021] Figure 2 illustrates a schematic representation of a calibration  
20 circuit 10. A voltage source 12 is coupled between two switched RC stages 14a-b. Each switched RC stage 14a-b comprises a resistive path with a resistor 16 of value R, which coupled to switch 18. Switch 18 is switched by control signal  $\Phi_D$ . A switched capacitive path is parallel to the resistive path. Switches 20a and 20b are coupled to either side of capacitor 22, having value C, and are switched by  
25  $\overline{\Phi_A}$  and  $\Phi_A$ , respectively. Switch 20a is coupled between one terminal of capacitor 22 and an input to operational amplifier 24 (for RC stage 14a, the

switch 20a is coupled to the inverting input of operational amplifier 24 and for RC stage 14b, the switch 20a is coupled to the non-inverting input of operational amplifier 24). Switch 20b is coupled between the other terminal of capacitor 22 and the voltage supply 12. A second pair of switches 26a and 26b are coupled between the respective terminals of capacitor 22 and ground. Switch 26a is controlled by control signal  $\Phi_A$  and switch 26b is controlled by control signal  $\overline{\Phi_A}$ . Accordingly, for each RC stage 14a-b, capacitor 22 will either be coupled between an input to operation amplifier 24 and ground or between the voltage supply 12 and ground, responsive to control signal  $\Phi_A$ .

10    **[0022]**       A capacitor 30 (having value  $C_0$ , which is equal to C for the embodiment described herein) in parallel with switch 32 (controlled by control signal  $\Phi_C$ ) is coupled between inverting input of operational amplifier 24 and the non-inverting differential output of operational amplifier 24. A capacitor 34 in parallel with switch 36 (also controlled by control signal  $\Phi_C$ ) is coupled  
15    between non-inverting input of operational amplifier 24 and the inverting differential output of operational amplifier 24. The inverting and non-inverting differential outputs of operational amplifier 24 are coupled to latch comparator 38. The output of latch comparator 38 is coupled to finite state machine 8.

20    **[0023]**       The operational amplifier 24 can be, for example, a Miller-compensated structure with NMOS input stage and NMOS output stage.

25    **[0024]**       The latch comparator 38 used in the calibration circuit is a fully differential implementation which doubles the input dynamic of the latch comparator (compared to a single ended solution) and thus reduces the problem of input offset. The fully differential solution acts like an amplification stage, thus reducing the complexity of the comparison stage.

[0025] The operation of the calibration circuit 10 is best described in connection with the timing diagram of Figure 3 and the schematic diagrams of Figures 4a-c, showing the calibration circuit in different stages of a calibration cycle.

5 [0026] Between times  $t_1$  and  $t_2$  in Figure 3, the calibration circuit is in reset mode, shown in Figure 4a. In this mode,  $\Phi_A$ ,  $\Phi_C$  and  $\Phi_D$  are all high. Thus, switches 18, 20b, 26a 32 and 36 are closed and switches 20a and 26b are open. Switch 32 shorts the terminals of capacitor 30 and switch 36 shorts the terminals of capacitor 34, hence, both capacitors 32 and 34 are discharged. Capacitors 22  
10 are charged to  $\pm V_{REF}$ .  $V_0$ , the differential output of the operational amplifier 24 is taken to its common mode output ( $V_{dd}/2$ , where  $V_{dd}$  is the power supply voltage to the operational amplifier). The time between  $t_1$  and  $t_2$  is  $P$  clocks.

[0027] Between times  $t_2$  and  $t_3$  in Figure 3, the calibration circuit is in integration mode, shown in Figure 4b. In this mode,  $\Phi_C$  transitions low while  
15  $\Phi_A$  and  $\Phi_D$  remain high. With  $\Phi_C$  low, switches 32 and 34 are open, allowing  $V_{REF}$  to charge the integrating capacitors 30 and 34 through resistors 16 (the charging of capacitor 30 is shown as a negatively sloping line and the charging of capacitor 34 is shown as a positively charging line). As can be seen in Figure 3, the rate of charging the capacitors 30 and 34 depends upon the RC product; a  
20 larger RC product results in a smaller slope. The integration mode lasts for  $2^N$  clocks.

[0028] During times  $t_3$  and  $t_5$  in Figure 3,  $\Phi_A$  is clocked and  $\Phi_D$  transitions low ( $\Phi_C$  remains low), as shown in Figure 4c. With  $\Phi_D$  low, the current path between the resistors 16 and capacitors 30 and 34 is removed. On  
25 each clock, when  $\Phi_A$  transitions low, the integrating capacitors 30 and 34 are

charged by an amount equal to  $V_{REF}$  (or  $-V_{REF}$ ). After  $P$  clocks ( $t_4$ ), a counter is reset in the FSM 8. From  $t_4$ ,  $2^N$  clocks are counted to  $t_5$ .

[0029] It is worth noting that, since the analog section of the filter calibration system is fully differential, the reference voltage is also a differential voltage, generated by means of a dedicated operational amplifier. In any case, for simplicity, all the following calculations are made in Single-Ended (SE). The dynamic required by the calibration system is  $[-2^N V_{REF} ; (2^N + P) V_{REF}]$ . In an actual design  $N=5$ ,  $P=16$  and  $V_{REF}=20\text{mV}$ ; thus the required dynamic results  $[-640\text{mV} ; 960\text{mV}]$  (SE) is thus well below the maximum dynamic of the operational amplifier.

[0030] In addition, the step of the positive-going staircase can be increased (up to  $30\text{mV}$ ), thus reducing the influence of the input-offset of the latch comparator. Of course, in this case the constant current producing the negative-going ramp is increased proportionally. Practically, this means increasing the gain of the preamplification stage in front of the latch comparator.

[0031] The state of the FSM's counter at the zero-crossing gives the measure of the RC product, which is designed with a nominal value that is  $4/3$  times the clock period  $T_C$  (the reason of this choice will be detailed later). The counter is reset at  $t_4$  ( $P$  clock periods after  $t_3$ ) and, with the binary weighted capacitor array designed according to Figure 1b, the code in the  $(2^N + P)$  state counter at the zero-crossing is just the one required to tune the filter to its nominal frequency response.

[0032] The control circuit parameters  $P$  and  $N$  are chosen according to (a) the expected processing spreads, (b) the required filter accuracy and (c) the maximum allowed calibration time. It can be demonstrated that this technique compensates processing spreads in the range  $\pm 100 / (1 + P / 2^{N-1})\%$  and produces a filter with an accuracy of  $\pm 50 / (P + 1)\%$ .



[0033] The calibration time ( $T_{CAL}$ ) is equal to  $T_{SU} + 2(P + 2^{N-1})T_C$ , where  $T_{SU}$  is a start-up time necessary to properly initialize the FSM. Assuming  $T_{SU}$  negligible, this means that doubling the accuracy of the algorithm means roughly doubling  $T_{CAL}$ .

- 5 [0034] For  $P = 16$  and  $2^N = 32$  (i.e.  $N=5$ ), the filter accuracy is set to less than 3% and allows a maximum RC product spread of  $\pm 50\%$  (sufficient for current day technologies with spreads of  $\pm 47\%$ ).

[0035] As previously stated, the default setting for the RC product is fixed to  $4/3T_C$ . This solution has been adopted to cover the full range of the RC product spreading. In fact, the voltage value at the output of the integrator at the  
10 end of the integration phase ( $t_2 - t_3$ ) results  $V_0 = V_{REF} 2^N \frac{1}{R^* C^* f_c}$ , where  $R^*$  and  $C^*$  are the resistor and the capacitor implemented in the design. If the maximum spread is  $\pm 50\%$  (as supposed), the value of  $V_0$  may vary from  $2/3V_0^*$  (i.e.,  $V_0^*/(1+0.5)$ ) up to  $2V_0^*$  (i.e.,  $V_0^*/(1-0.5)$ ), where  $V_0^*$  is the value of the integrated  
15 voltage with ideal conditions. This means that there is an asymmetry in the integrated voltage between the positive and the negative spread. Thus, if the RC product is equal to  $T_C$ , there is no chance to correct the case when the integration voltage results  $2V_0^*$ .

- [0036] The calibration range results in this case  $[-33\% ; +100\%]$ . In fact, for  
20 RC changes in the range  $\pm 50\%$ , C array will cover  $\pm(1/50\%)$ , which is  $[-33\% ; +100\%]$ . If the RC product is set to  $4/3T_C$ , the voltage range at the output of

the integrator results  $[1/2 V_0^* ; -3/2 V_0^*]$  (i.e.  $\left[ \frac{V_0^*}{\frac{4}{3}(1+0.5)} ; \frac{-V_0^*}{\frac{4}{3}(1-0.5)} \right]$ ) and this

allows to perform the calibration covering the full range. Of course, in this case,

there is an asymmetry in the nominal case digital code, which controls the capacitor array.

[0037] The code can be calculated as follows. Using  $\frac{1}{\left(1 \pm \frac{x_{1,2}}{100}\right)}$  as the

coverage of the calibration algorithm, where  $x_{1,2}$  are the minimum and maximum spread of the RC product, and this range has to be  $\pm 50\%$ , the corresponding range of variation of the RC product can be calculated as:

$$\frac{1}{\left(1 - \frac{x_1}{100}\right)} = \frac{100}{100 - x_1} = \frac{100}{66} \quad (+50\%) \Rightarrow x_1 = 33 \quad (-33\%)$$

$$\frac{1}{\left(1 + \frac{x_2}{100}\right)} = \frac{100}{100 + x_2} = \frac{100}{200} \quad (-50\%) \Rightarrow x_2 = 100 \quad (+100\%)$$

Accordingly, a symmetrical correction range needs an asymmetrical correction code for the nominal case.

[0038] Thus, in the first case, no spread gives the code 10000 (assuming  $N=5$ ), while in the second case, in the same condition, the driving code will be 01000 (since the RC product is greater than  $T_C$ ). With this configuration, the maximum RC product (which corresponds to  $1/2 V_0^*$ ) will give the minimum digital code (00000), while the minimum RC product ( $3/2 V_0^*$ ) will give the maximum digital code (11111).

[0039] Figure 5 shows the behavior of the calibration system in all the tuning conditions ( $RC_{MIN}$ ,  $RC_{NOM}$ ,  $RC_{MAX}$ ). In analyzing the nominal case and the limits of the calibration range,  $V_{p\_diff\_NOM}$  (the differential output voltage of the integrator at the end of the integration phase in the nominal case) is defined

as  $\frac{V_{REF} 2^N T_{CK}}{\frac{4}{3} RC}$ . The following relationship gives the value of the output code

since it calculates the number of discharging steps by equating the integrated voltage on the integrator capacitor with the product of the single discharging step by the number of steps required to completely discharge the capacitor.

$$\frac{V_{REF} 2^N T_{CK}}{\frac{4}{3} RC} = \frac{V_{REF} C_1 (n_{NOM} + P)}{C_0}, \text{ where } T_{CK}=RC \text{ and } C_1=C_0;$$

$$\frac{2^N}{\frac{4}{3}} = n_{NOM} + P; \text{ and}$$

$$n_{NOM} = 3 \times 2^{N-2} - P.$$

[0040] With N=5 and P=16 (as in the illustrated case),  $n_{NOM}=8$  and thus the corresponding digital code for the switches is 01000.

[0041] The same operation can be performed both for the maximum and minimum RC product. For the maximum RC product:

$$V_{p\_diff\_MAX} = \frac{V_{REF} 2^N T_{CK}}{2RC};$$

$$\frac{V_{REF} 2^N T_{CK}}{2RC} = \frac{V_{REF} C_1 (n_{MAX} + P)}{C_0}, \text{ where } T_{CK}=RC \text{ and } C_1=C_0; \text{ and}$$

$$n_{MAX} = 2^{N-1} - P.$$

Thus,  $n_{MAX}=0$  and then the corresponding digital code for the switches is 00000.

[0042] For the minimum RC product:

$$V_{p\_diff\_MIN} = \frac{V_{REF} 2^N T_{CK}}{\frac{2}{3} RC};$$

$$\frac{V_{REF} 2^N T_{CK}}{\frac{2}{3} RC} = \frac{V_{REF} C_1 (n_{MIN} + P)}{C_0}, \text{ where } T_{CK}=RC \text{ and } C_1=C_0; \text{ and}$$

$$\frac{2^N}{\frac{2}{3}} = n_{MIN} + P.$$

Thus,  $n_{MIN}=32$  and then the corresponding digital code for the switches is 11111.

[0043] In summary, by setting  $RC=4/3T_C$ , it is possible to cover the whole spreading range of  $\pm 47\%$  for a current processing technology.

5 [0044] Figure 6 shows the timing for the FSM 8. The FSM 8 is activated by an external signal (CAL); after  $T_{CAL}$ , the filter calibration is performed, the digital code is stored in a register and then, a signal (EOC, End Of Calibration, active high) is delivered to the control block. Thus, the calibration system goes automatically in power-off mode, ready for another calibration operation. When  
10 CAL goes down also EOC is set to '0'.

[0045] The calibration system 10 presents a fully differential architecture instead of a single ended solution as proposed in *Hughes*. This choice has been made, even if the architecture of the integrator is more complicated, since it doubles the number of passive elements (R, C) and requires a fully differential  
15 operational amplifier, because it allows simplification of the architecture of the latch comparator, since the fully differential solution acts like a pre-amplification stage for the comparison stage. Thus a simple latch comparator, without any pre-amplification stage, can be used.

[0046] From an area point of view, the two solutions are comparable, but  
20 the fully differential solution proposed herein presents some key advantages: (1) the result of the calibration process is independent from any error in the reference signals (both for the integrator and for the latch comparator), and (2) the clock-feedthrough and the charge injection caused by the switches in the switched capacitor integrator does not influence the result. It is worth noting that

in this case no delayed phases have to be used since the input signal (reference voltage) is constant.

[0047] Figure 7 illustrates a Butterworth RC filter that could be used as the RC filter 6 in Figure 1a. In Figure 7, a differential input (IN) is coupled to the inverting and non-inverting inputs of a differential operational amplifier 40 through resistors 42 and 44, respectively. Resistor 46 and tunable capacitor 48 are coupled between the inverting input and non-inverting output of the operational amplifier 40. Resistor 50 and tunable capacitor 52 are coupled between the non-inverting input and inverting output of the operational amplifier 40. The non-inverting output of operational amplifier 40 is coupled to the non-inverting output of operational amplifier 54 through resistor 56. The inverting output of operational amplifier 40 is coupled to the inverting input output of operational amplifier 54 through resistor 58. Tunable capacitor 60 is coupled between the inverting input and non-inverting output of operational amplifier 54. Tunable capacitor 62 is coupled between the non-inverting input and inverting output of operational amplifier 54. Resistor 64 is coupled between the inverting input of operational amplifier 40 and the non-inverting output of operational amplifier 54. Resistor 66 is coupled between the non-inverting input of operational amplifier 40 and the inverting output of operational amplifier 54. The non-inverting output of operational amplifier 54 is coupled to the inverting input of operational amplifier 68 through resistor 70. The inverting output of operational amplifier 54 is coupled to the non-inverting input of operational amplifier 68 through resistor 72. Resistor 74 and tunable capacitor 76 are coupled between the inverting input and non-inverting output of operational amplifier 68. Resistor 78 and tunable capacitor 80 are coupled between the non-inverting input and inverting output of operational amplifier 68. Operational amplifier 68 provides the filter differential output (OUT).

[0048] The tunable capacitors of the filter are made adjustable by using programmable binary-weighted capacitor arrays, as shown in Figure 1b, which are designed to have nominal center values equal to the design values (C). The range of these capacitors should be at least as great as the combined spreads of resistors and capacitors (approximately  $\pm 50\%$ ). Tuning is achieved by supplying the appropriate digital code to the arrays as calculated by the finite state machine 8.

[0049] The number of bits composing the code driving each capacitor array 7 (and hence the resolution of the capacitor array 7) determines the accuracy of the calibration; it is worth noting that this number influences also the calibration time. In other words, this means that increasing the filter accuracy means increasing the calibration time: in particular, one more bit means doubling the time required for the calibration. The choice of the code length is then a trade-off between these two issues.

15 [0050] Although the Detailed Description of the invention has been directed to certain exemplary embodiments, various modifications of these embodiments, as well as alternative embodiments, will be suggested to those skilled in the art. The invention encompasses any modifications or alternative embodiments that fall within the scope of the Claims.